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Our Docket No.: 0325.00239

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Risto D. Bell et al.		
Application No.:	09/410,160	Examiner:	Garcia Otero, E.
Filed:	September 30, 1999	Art Group:	2123
For:	METHOD AND APPARATUS FOR AUTOMATED ENUMERATION, SIMULATION, IDENTIFICATION AND/OR IRRADIATION OF DEVICE ATTRIBUTES		

I hereby certify that this letter, the response or amendment attached hereto are being deposited with the United States Postal Service as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on February 22, 2005 .

By: Mary Donna Berkley
Mary Donna Berkley

SUPPLEMENTAL REPLY BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Appellants submit the following Supplemental Reply Brief pursuant to 37 C.F.R. §41.41 for consideration by the Board of Patent Appeals and Interferences.

STATUS OF CLAIMS

Claims 1-20 are pending and remain rejected only under new grounds of rejection raised for the first time in the Supplemental Examiner's Answer. The Examiner has withdrawn all prior 35 U.S.C. §103 and §112 rejections on which the original appeal was based.[1] Appellants request that the appeal of claims 1-20 be maintained in view of the following arguments.

ISSUES

The first new issue is whether claims 1, 2, 12, 13, 18 and 19 are patentable under 35 U.S.C. §103(a) over Kablanian et al., U.S. Patent No. 5,764,878, (hereafter Kablanian) in view of Tzori, U.S. Patent No. 6,202,044.

The second new issue is whether claims 3-7, 14-16 and 20 are patentable under 35 U.S.C. §103(a) over Kablanian in view of Tzori and Sample et al., U.S. Patent No. 5,841,967, (hereafter Sample).

The third new issue is whether claims 8-11 and 17 are patentable under 35 U.S.C. §103(a) over Kablanian in view of Tzori, Sample and Higgins et al., U.S. Patent No. 6,397,349, (hereafter Higgins).

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[1] Supplemental Examiner's Answer, page 5, lines 4-5.

ARGUMENTS IN RESPONSE TO SUPPLEMENTAL EXAMINER'S ANSWER

Appellants thank the Examiner for withdrawing all prior 35 U.S.C. §103 and §112 rejections.[2]

A. New Grounds of Rejection

Appellants assert that the new grounds of rejection in the Supplemental Examiner's Answer are improper under 37 C.F.R. §41, subpart B and thus should be withdrawn. 37 C.F.R. §41.50(a)(2) states:

> (2) If a supplemental examiner 's answer is written in response to a remand by the Board for further consideration of a rejection pursuant to paragraph (a)(1) of this section, the appellant must within two months from the date of the supplemental examiner 's answer **exercise one of the following two options** to avoid sua sponte dismissal of the appeal as to the claims **subject to the rejection for which the Board has remanded the proceeding**: (i) Reopen prosecution...[or] (ii) Maintain appeal. (Emphasis added)

Furthermore, page 24 of the slide set "Final Rule Making on Practice Before the Board of Patent Appeals and Interferences (BPAI)" posted on the U.S. Patent and Trademark website September 16, 2004 states:

> If a supplemental examiner's answer is written after a BPAI remand, appellant may request that prosecution be reopened pursuant to § 41.50(a)(2) if:
> 1. The remand by the Board is for further consideration of a rejection; and
> 2. The date of the remand is on or after the September 13, 2004.
> Appellant may **not** request that prosecution be reopened:
> 1. **If the Board remands the application prior to September 13, 2004**; or
> 2. If the Board remands the application for a reason other than for further consideration of a rejection. (Emphasis added)

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[2] Supplemental Examiner's Answer, page 5, lines 4-5.

The remand from the Board took place on August 19, 2004. The remand date appears to eliminate the Appellants' option to request reopening of prosecution. Appellants only remaining option under 37 C.F.R. §41.50(a)(2) appears to be to maintain the appeal **"as to the claims subject to the rejection for which the Board has remanded the proceeding."** Since the Appellants appear to be limited to arguing the original grounds of rejection remanded by the Board, the Supplemental Examiner's Answer would logically be likewise limited to the same original grounds. Allowing the Examiner to introduce 100% new grounds of rejection in the current situation where (i) Appellants appear to lack an opportunity to amend or introduce new evidence, (ii) Appellants appear to have no opportunity to request reopening of prosecution and (iii) Appellants did not originally seek the appeal based on the new grounds of rejection, would appear to give the Examiner an extremely unfair advantage and thus appears to be an improbable interpretation of 37 C.F.R. §41.51(a)(2).

Assuming, *arguendo*, that the Supplemental Examiner's Answer was written in response to Appellants' Reply Brief, the Supplemental Examiner's Answer is not compliant with 37 C.F.R. §41.43. In particular 37 C.F.R. §41.43(a)(2) states:

> (2) A supplemental examiner 's answer responding to a reply brief may not include a new ground of rejection.

The Examiner is expressly prohibited from including new grounds of rejection in a Supplemental Examiner's Answer. As such, the new grounds of rejection in the Supplemental Examiner's Answer appear to be improper under 37 C.F.R. §41, subpart B and should be withdrawn.

B. New Rejections under 35 U.S.C. § 103

The following remarks are made assuming, *arguendo*, that the new grounds of rejection in the Supplemental Examiner's Answer may somehow be procedurally proper.

1. Rejections over Kablanian in view of Tzori

a. Claims 1 and 2 are fully patentable over Kablanian and Tzori

Claim 1 provides a step for generating an enumeration of a plurality of fuses in a design. The Examiner asserts that Kablanian discloses the claimed step for generating as follows:[3]

> External software is used to determine optimal utilization of the redundant memory lines to repair defective memory lines. The third process is the repair process. Fuse and/or antifuse equipment facilitates severing circuit fuses that are formed on the chip for selective removal through convention laser beam techniques to repair a defective memory cell.[4]

Nowhere in the above text does Kablanian appear to discuss a step for **generating an enumeration** of a plurality of fuses in a design as presently claimed. Furthermore, the Examiner fails to provide any evidence or convincing line of reasoning why one of ordinary skill in the art would interpret the above text as teaching the claim limitations. Therefore, *prima facie* obviousness has not been established for lack of evidence that the references teach all of the claim limitations.

Claim 1 further provides a step for simulating a design with at least one of a plurality of fuses programmed for a repair to verify the repair. The Examiner asserts that the claimed step is discussed by Tzori as follows:[5]

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[3] Supplemental Examiner's Answer, page 6, last 5 lines.

[4] Kablanian, column 2, lines 5-11.

[5] Supplemental Examiner's Answer, page 7, lines 2-8.

> Performing a Verilog simulation requires that a digital logic designer employ a computer program model for the system by aggregating into a simulation computer program various software modules.[6]

Nowhere in the above text does Tzori appear to discuss simulating a design with at least one of a plurality of fuses programmed for a repair to verify the repair as presently claimed. Furthermore, the Examiner fails to provide any evidence or convincing line of reasoning why one of ordinary skill in the art would interpret the above text as teaching the claim limitations. Therefore, *prima facie* obviousness has not been established for lack of evidence that the references teach all of the claimed limitations.

Furthermore, the Examiner fails to provide clear and particular evidence of motivation to combine the references. The asserted motivation for "using 'External software' in order to 'determined the optimal utilization' "[7] does not appear to explain why one of ordinary skill in the art would select Tzori to combine with Kablanian in the absence of the teachings of the application. In particular, the Examiner appears to admit that the "external software" of Kablanian could be any "standard commercial simulation software,"[8] not the particular software mentioned in Tzori. Furthermore, the Examiner uses the same alleged motivation to combine Kablanian with all of the references used in the rejections suggesting that the alleged motivation is neither clear nor particular.[9] Therefore, the Examiner has failed to meet the burden of factually establishing a *prima*

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[6] Tzori, column 1, lines 28-31.

[7] Supplemental Examiner's Answer, page 7, lines 17-19.

[8] Supplemental Examiner's Answer, page 7, line 21.

[9] Supplemental Examiner's Answer, see "At the time" paragraphs on pages 7-17, 19-24 and 26.

facie case of obviousness. Claim 2 depends from claim 1. As such, the rejection of claims 1 and 2 should be reversed.

b. Claim 12 is fully patentable over Kablanian and Tzori

Claim 12 provides a first circuit and a second circuit. In contrast, the Examiner provides no evidence or arguments that the proposed combination of Kablanian and Tzori teach or suggest a first circuit and a second circuit as presently claimed. As such, *prima facie* obviousness has not been established for lack of evidence that the references teach all of the claim limitations.

Claim 12 further provides that the first circuit is configured to enumerate a plurality of fuses in a design. The Examiner asserts that the claimed first circuit is discussed by Kablanian as follows:[10]

> External software is used to determine optimal utilization of the redundant memory lines to repair defective memory lines. The third process is the repair process. Fuse and/or antifuse equipment facilitates severing circuit fuses that are formed on the chip for selective removal through convention laser beam techniques to repair a defective memory cell.[11]

Nowhere in the above text does Kablanian appear to discuss a first circuit configured to **enumerate** a plurality of fuses in a design as presently claimed. Furthermore, the Examiner fails to provide any evidence or convincing line of reasoning why one of ordinary skill in the art would interpret the above text as teaching the claim limitations. Therefore, *prima facie* obviousness has not been established for lack of evidence that the references teach all of the claim limitations.

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[10] Supplemental Examiner's Answer, page 6, last 5 lines.

[11] Kablanian, column 2, lines 5-11.

Claim 12 further provides that the second circuit is configured to simulate a design with at least one of a plurality of fuses programmed for a repair to verify the repair. The Examiner asserts that the claimed second circuit is discussed by Tzori as follows:[12]

> Performing a Verilog simulation requires that a digital logic designer employ a computer program model for the system by aggregating into a simulation computer program various software modules.[13]

Nowhere in the above text does Tzori appear to discuss a second circuit configured to simulate a design with at least one of a plurality of fuses programmed for a repair to verify the repair as presently claimed. Furthermore, the Examiner fails to provide any evidence or convincing line of reasoning why one of ordinary skill in the art would interpret the above text as teaching the claim limitations. Therefore, *prima facie* obviousness has not been established for lack of evidence that the references teach all of the claim limitations.

Furthermore, the Examiner fails to provide clear and particular evidence of motivation to combine the references. The asserted motivation for "using 'External software' in order to 'determined the optimal utilization' "[14] does not appear to explain why one of ordinary skill in the art would select Tzori to combine with Kablanian in the absence of the teachings of the application. In particular, the Examiner appears to admit that the "external software" of Kablanian could be any "standard commercial simulation software,"[15] not the particular software mentioned

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[12] Supplemental Examiner's Answer, page 7, lines 2-8.

[13] Tzori, column 1, lines 28-31.

[14] Supplemental Examiner's Answer, page 7, lines 17-19.

[15] Supplemental Examiner's Answer, page 7, line 21.

in Tzori. Furthermore, the Examiner uses the same alleged motivation to combine Kablanian with all of the references used in the rejections suggesting that the alleged motivation is neither clear nor particular.[16] Therefore, the Examiner has failed to meet the burden of factually establishing a *prima facie* case of obviousness. As such, the rejection of claim 12 should be reversed.

c. Claims 13 is fully patentable over Kablanian and Tzori

Claim 13 provides a means for generating, a means for compiling and a means for simulating. In contrast, the Examiner provides no evidence or argument that the proposed combination of Kablanian and Tzori teach or suggest a means for generating, a means for compiling and a means for simulating as presently claimed. As such, *prima facie* obviousness has not been established for lack of evidence that the references teach all of the claim limitations.

Claim 13 further provides a means for generating an enumeration of a plurality of fuses in a design. The Examiner asserts that the claimed means for generating is discussed by Kablanian as follows:[17]

> External software is used to determine optimal utilization of the redundant memory lines to repair defective memory lines. The third process is the repair process. Fuse and/or antifuse equipment facilitates severing circuit fuses that are formed on the chip for selective removal through convention laser beam techniques to repair a defective memory cell.[18]

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[16] Supplemental Examiner's Answer, see "At the time" paragraphs on pages 7-17, 19-24 and 26.

[17] Supplemental Examiner's Answer, page 6, last 5 lines.

[18] Kablanian, column 2, lines 5-11.

Nowhere in the above text does Kablanian appear to discuss a means for **generating an enumeration** of a plurality of fuses in a design as presently claimed. Furthermore, the Examiner fails to provide any evidence or convincing line of reasoning why one of ordinary skill in the art would interpret the above text as teaching the claim limitations. Therefore, *prima facie* obviousness has not been established for lack of evidence that the references teach all of the claim limitations.

Claim 13 further provides a means for simulating a design with at least one of a plurality of fuses programmed for a repair to verify the repair. The Examiner asserts that the claimed means for simulating is discussed by Tzori as follows:[19]

> Performing a Verilog simulation requires that a digital logic designer employ a computer program model for the system by aggregating into a simulation computer program various software modules.[20]

Nowhere in the above text does Tzori appear to discuss a means for simulating a design with at least one of a plurality of fuses programmed for a repair to verify the repair as presently claimed. Furthermore, the Examiner fails to provide any evidence or convincing line of reasoning why one of ordinary skill in the art would interpret the above text as teaching the claim limitations. Therefore, *prima facie* obviousness has not been established for lack of evidence that the references teach all of the claimed limitations.

Furthermore, the Examiner fails to provide clear and particular evidence of motivation to combine the references. The asserted motivation for "using 'External software' in

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[19] Supplemental Examiner's Answer, page 7, lines 2-8.

[20] Tzori, column 1, lines 28-31.

order to 'determined the optimal utilization' "[21] does not appear to explain why one of ordinary skill in the art would select Tzori to combine with Kablanian in the absence of the teachings of the application. In particular, the Examiner appears to admit that the "external software" of Kablanian could be any "standard commercial simulation software,"[22] not the particular software mentioned in Tzori. Furthermore, the Examiner uses the same alleged motivation to combine Kablanian with all of the references used in the rejections suggesting that the alleged motivation is neither clear nor particular.[23] Therefore, the Examiner has failed to meet the burden of factually establishing a *prima facie* case of obviousness. As such, the rejection of claim 13 should be reversed.

d. Claims 18 is fully patentable over Kablanian and Tzori

Claim 18 depends from claim 12 and thus contains all of the limitations of claim 12. Consequently, the arguments presented above in support of the patentability of claim 12 are incorporated hereunder in support of claim 18.

Claim 18 further provides a first circuit configured to provide an elevation of fuses at least one level of abstraction in a design. The Examiner asserts that Tzori teaches the claimed first circuit as follows:[24]

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[21] Supplemental Examiner's Answer, page 7, lines 17-19.

[22] Supplemental Examiner's Answer, page 7, line 21.

[23] Supplemental Examiner's Answer, see "At the time" paragraphs on pages 7-17, 19-24 and 26.

[24] Supplemental Examiner's Answer, page 23, lines 11-17.

> Performing a Verilog simulation requires that a digital logic designer employ a computer program model for the system by aggregating into a simulation computer program various software modules. The software modules making up a Verilog model include modules for each digital logic circuit included in the simulation, for specifying interconnections among the Verilog logic circuit modules, and for specifying timing relationships among the interconnected Verilog logic circuit modules.[25]

Nowhere in the above text does Tzori appear to discuss a first circuit configured to provide an elevation of fuses at least one level of abstraction in a design as presently claimed. Furthermore, the Examiner fails to provide any evidence or convincing line of reasoning why one of ordinary skill in the art would interpret the above text as teaching the claim limitations. Therefore, *prima facie* obviousness has not been established for lack of evidence that the references teach or suggest all of the claim limitations.

Furthermore, Appellants' representative respectfully traverses the assertion by the Examiner that Verilog inherently contains at least one level of abstraction.[26] MPEP §2112 states:

> "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." *Ex parte Levy* 17 USPQ2d 1461, 1464, 1464 (Bd. Pat. App. & Inter. 1990)(emphasis in original)

However, no evidence or convincing line of reasoning has been provided by the Examiner why at least one level of abstraction necessarily results from the existence of Verilog. Therefore, inherency has not been established. As such, the rejection of claim 18 should be reversed.

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[25] Tzori, column 1, lines 28-36.

[26] Supplemental Examiner's Answer, page 23, line 18.

e. Claims 19 is fully patentable over Kablanian and Tzori

Claim 19 depends from claim 12 and thus contains all of the limitations of claim 12. Consequently, the arguments presented above in support of the patentability of claim 12 are incorporated hereunder in support of claim 19.

Claim 19 further provides a first circuit configured to collect data relevant to a plurality of fuses that are grouped. The Examiner asserts that Tzori teaches the claimed first circuit as follows:[27]

> Performing a Verilog simulation requires that a digital logic designer employ a computer program model for the system by aggregating into a simulation computer program various software modules. The software modules making up a Verilog model include modules for each digital logic circuit included in the simulation, for specifying interconnections among the Verilog logic circuit modules, and for specifying timing relationships among the interconnected Verilog logic circuit modules.[28]

Nowhere in the above text does Tzori appear to discuss a first circuit configured to collect data relevant to a plurality of fuses that are grouped as presently claimed. Furthermore, the Examiner fails to provide any evidence or convincing line of reasoning why one of ordinary skill in the art would interpret the above text as teaching the claim limitations. Therefore, *prima facie* obviousness has not been established for lack of evidence that the references teach or suggest all of the claim limitations. As such, the rejection of claim 19 should be reversed.

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[27] Supplemental Examiner's Answer, page 24, lines 19-24.

[28] Tzori, column 1, lines 28-36.

2. Rejections over Kablanian in view of Tzori and Sample

The Examiner fails to provide clear and particular evidence of motivation to combine the references. The asserted motivation for "using 'External software' in order to 'determined the optimal utilization' "[29] does not appear to explain why one of ordinary skill in the art would select both Tzori and Sample to combine with Kablanian in the absence of the teachings of the application. Furthermore, the Examiner uses the same alleged motivation to combine Kablanian with all of the references used in the rejections suggesting that the alleged motivation is neither clear nor particular.[30] Therefore, the Examiner has failed to meet the burden of factually establishing a *prima facie* case of obviousness. As such, the rejections of claims 3-7, 14-16 and 20 should be reversed.

a. Claims 14 and 3 are fully patentable over Kablanian, Tzori and Sample

Claim 14 depends from claim 1 and thus contains all of the limitations of claim 1. Consequently, the arguments presented above in support of the patentability of claim 1 are incorporated hereunder in support of claim 14.

Claim 14 further provides that data compiled for each of a plurality of fuses comprises schematic path data. The Examiner asserts that (i) a Netlist Generator block 140 and a "Part, Place, Route" block 148 in FIG. 13 and (ii) a phrase "the transistor list of layout specification is used to bu[rn] fuses" of Sample teach the claim limitations.[31] In contrast, the blocks 140 and 148 in FIG.

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[29] Supplemental Examiner's Answer, first occurrence on page 9, lines 16-19.

[30] Supplemental Examiner's Answer, see "At the time" paragraphs on pages 7-17, 19-24 and 26.

[31] Supplemental Examiner's Answer, page 19, lines 3-5.

13 of Sample and the above quoted phrase from Sample appear to be silent regarding data compiled for each of a plurality of fuses comprising schematic path data as presently claimed. Furthermore, the Examiner fails to provide any evidence or convincing line of reasoning why one of ordinary skill in the art would interpret the above blocks and phrase as teaching the claim limitations. Therefore, *prima facie* obviousness has not been established for lack of evidence that the references teach all of the claim limitations. Claim 3 depends from claim 14. As such, the rejection of claims 14 and 3 should be reversed.

b. Claim 4 is fully patentable over Kablanian, Tzori and Sample

Claim 4 depends from claim 1 and thus contains all of the limitations of claim 1. Consequently, the arguments presented above in support of the patentability of claim 1 are incorporated hereunder in support of claim 4.

Claim 4 further provides a sub-step for generating a list of layout coordinates and paths in the design as part of (from claim 1) a step of compiling data for each of a plurality of fuses. The Examiner asserts that (i) a Netlist Generator block 140 and a "Part, Place, Route" block 148 in FIG. 13 of Sample and (ii) a phrase "the transistor list of layout specification is used to bu[rn] fuses" of Sample teach the claimed sub-step for generating a list.[32] In contrast, the blocks 140 and 148 in FIG. 13 of Sample and the above quoted phrase from Sample appear to be silent regarding a step for generating a list of layout coordinates and paths in a design as part of a step of compiling data for each of a plurality of fuses as presently claimed. Furthermore, the Examiner fails to provide any

[32] Supplemental Examiner's Answer, page 10, lines 15-18.

evidence or convincing line of reasoning why one of ordinary skill in the art would interpret the above blocks and phrase as teaching the claim limitations. Therefore, *prima facie* obviousness has not been established for lack of evidence that the references teach all of the claim limitations. As such, the rejection of claim 4 should be reversed.

c. Claim 5 is fully patentable over Kablanian, Tzori and Sample

Claim 5 depends from claim 1 and thus contains all of the limitations of claim 1. Consequently, the arguments presented above in support of the patentability of claim 1 are incorporated hereunder in support of claim 5.

Claim 5 further provides a step for generating a fuse report. The Examiner asserts that (i) a Netlist Generator block 140 and a "Part, Place, Route" block 148 in FIG. 13 of Sample and (ii) a phrase "the transistor list of layout specification is used to bu[rn] fuses" of Sample teach the claimed generating step.[33] In contrast, the blocks 140 and 148 in FIG. 13 of Sample and the above quoted phrase from Sample appear to be silent regarding a step for generating a fuse report as presently claimed. Furthermore, the Examiner fails to provide any evidence or convincing line of reasoning why one of ordinary skill in the art would interpret the above blocks and phrase as teaching the claim limitations. Therefore, *prima facie* obviousness has not been established for lack of evidence that the references teach all of the claim limitations. As such, the rejection of claim 5 should be reversed.

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[33] Supplemental Examiner's Answer, page 11, lines 14-16.

d. Claim 6 is fully patentable over Kablanian, Tzori and Sample

Claim 6 depends from claim 5 and thus contains all of the limitations of claim 5. Consequently, the arguments presented above in support of the patentability of claim 5 are incorporated hereunder in support of claim 6.

Claim 6 further provides a step for listing physical locations of a device in a design in response to a fuse report. The Examiner asserts that (i) a Netlist Generator block 140 and a "Part, Place, Route" block 148 in FIG. 13 of Sample and (ii) a phrase "the transistor list of layout specification is used to bu[rn] fuses" of Sample teach the claimed step for listing.[34] In contrast, the blocks 140 and 148 in FIG. 13 of Sample and the above quoted phrase from Sample appear to be silent regarding a step for listing physical locations of a device in a design in response to a fuse report as presently claimed. Furthermore, the Examiner fails to provide any evidence or convincing line of reasoning why one of ordinary skill in the art would interpret the above blocks and phrase as teaching the claim limitations. Therefore, *prima facie* obviousness has not been established for lack of evidence that the references teach all of the claim limitations. As such, the rejection of claim 6 should be reversed.

e. Claim 7 is fully patentable over Kablanian, Tzori and Sample

Claim 7 depends from claim 1 and thus contains all of the limitations of claim 1. Consequently, the arguments presented above in support of the patentability of claim 1 are incorporated hereunder in support of claim 7.

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[34] Supplemental Examiner's Answer, page 12, lines 13-16.

Claim 7 further provides a step for generating a repair file that predicts at least one of a plurality of fuses programmed for a repair. The Examiner asserts that (i) a Netlist Generator block 140 and a "Part, Place, Route" block 148 in FIG. 13 of Sample and (ii) a phrase "the transistor list of layout specification is used to bu[rn] fuses" of Sample teach the claimed step for generating a repair file.[35] In contrast, the blocks 140 and 148 in FIG. 13 of Sample and the above quoted phrase from Sample appear to be silent regarding a step for generating a repair file as presently claimed. Furthermore, the Examiner fails to provide any evidence or convincing line of reasoning why one of ordinary skill in the art would interpret the above blocks and phrase as teaching the claim limitations. Therefore, *prima facie* obviousness has not been established for lack of evidence that the references teach all of the claim limitations. As such, the rejection of claim 7 should be reversed.

f. Claim 15 is fully patentable over Kablanian, Tzori and Sample

Claim 15 depends from claim 1 and thus contains all of the limitations of claim 1. Consequently, the arguments presented above in support of the patentability of claim 1 are incorporated hereunder in support of claim 15.

Claim 15 further provides that (from claim 1) data compiled for a plurality of fuses (from claim 15) comprises physical location data. The Examiner asserts that (i) a Netlist Generator block 140 and a "Part, Place, Route" block 148 in FIG. 13 of Sample and (ii) a phrase "the transistor list of layout specification is used to bu[rn] fuses" of Sample teach the claim limitation.[36] In contrast,

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[35] Supplemental Examiner's Answer, page 13, lines 13-16.

[36] Supplemental Examiner's Answer, page 20, lines 5-7.

the blocks 140 and 148 in FIG. 13 of Sample and the above quoted phrase from Sample appear to be silent regarding data compiled for a plurality of fuses comprising physical location data as presently claimed. Furthermore, the Examiner fails to provide any evidence or convincing line of reasoning why one of ordinary skill in the art would interpret the above blocks and phrase as teaching the claim limitations. Therefore, *prima facie* obviousness has not been established for lack of evidence that the references teach all of the claim limitations. As such, the rejection of claim 15 should be reversed.

g. Claim 16 is fully patentable over Kablanian, Tzori and Sample

Claim 16 depends from claim 1 and thus contains all of the limitations of claim 1. Consequently, the arguments presented above in support of the patentability of claim 1 are incorporated hereunder in support of claim 16.

Claim 16 further provides a step for mapping a plurality of co-ordinates of a plurality of fuses to a plurality of verilog program statements. The Examiner asserts that (i) a Netlist Generator block 140 and a "Part, Place, Route" block 148 in FIG. 13 of Sample and (ii) a phrase "the transistor list of layout specification is used to bu[rn] fuses" of Sample teach the claimed step for mapping.[37] In contrast, the blocks 140 and 148 in FIG. 13 of Sample and the above quoted phrase from Sample appear to be silent regarding a step for mapping a plurality of co-ordinates of a plurality of fuses to a plurality of verilog program statements as presently claimed. Furthermore, the Examiner fails to provide any evidence or convincing line of reasoning why one of ordinary skill in

[37] Supplemental Examiner's Answer, page 20, lines 5-7.

the art would interpret the above blocks and phrase as teaching the claim limitations. Therefore, *prima facie* obviousness has not been established for lack of evidence that the references teach all of the claim limitations. As such, the rejection of claim 16 should be reversed.

h. Claim 20 is fully patentable over Kablanian, Tzori and Sample

Claim 20 depends from claim 12 and thus contains all of the limitations of claim 12. Consequently, the arguments presented above in support of the patentability of claim 12 are incorporated hereunder in support of claim 20.

Claim 20 further provides a second circuit configured to write a report file. The Examiner asserts that (i) a Netlist Generator block 140 and a "Part, Place, Route" block 148 in FIG. 13 of Sample and (ii) a phrase "the transistor list of layout specification is used to bu[rn] fuses" of Sample teach the claimed second circuit.[38] In contrast, the blocks 140 and 148 in FIG. 13 of Sample and the above quoted phrase from Sample appear to be silent regarding a second circuit configured to write a report file as presently claimed. Furthermore, the Examiner fails to provide any evidence or convincing line of reasoning why one of ordinary skill in the art would interpret the above blocks and phrase as teaching the claim limitations. Therefore, *prima facie* obviousness has not been established for lack of evidence that the references teach all of the claim limitations. As such, the rejection of claim 20 should be reversed.

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[38] Supplemental Examiner's Answer, page 25, lines 24-27.

3. Rejections over Kablanian in view of Tzori, Sample and Higgins

The Examiner fails to provide clear and particular evidence of motivation to combine the references. The asserted motivation for "using 'External software' in order to 'determined the optimal utilization' "[39] does not appear to explain why one of ordinary skill in the art would select all three of Tzori, Sample and Higgins to combine with Kablanian in the absence of the teachings of the application. Furthermore, the Examiner uses the same alleged motivation to combine Kablanian with all of the references used in the rejections suggesting that the alleged motivation is neither clear nor particular.[40] Therefore, the Examiner has failed to meet the burden of factually establishing a *prima facie* case of obviousness. As such, the rejections of claims 8-11 and 17 should be reversed.

a. Claims 8 and 9 are fully patentable over Kablanian, Tzori, Sample and Higgins

Claim 8 depends from claim 7 and thus contains all of the limitations of claim 7. Consequently, the arguments presented above in support of the patentability of claim 7 are incorporated hereunder in support of claim 8.

Claim 8 further provides a step for creating a repair program in response to a repair file. The Examiner asserts that Higgins teaches the claimed creating step as follows:[41]

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[39] Supplemental Examiner's Answer, first occurrence on page 14, lines 16-19.

[40] Supplemental Examiner's Answer, see "At the time" paragraphs on pages 7-17, 19-24 and 26.

[41] Supplemental Examiner's Answer, page 14, lines 13-15.

> Location information is then supplied to a controller for a laser repair device, which achieves a hardware fix.[42]

Nowhere in the above text does Higgins appear to discuss creating a repair program as presently claimed. Furthermore, the Examiner fails to provide any evidence or convincing line of reasoning why one of ordinary skill in the art would interpret the above text as teaching the claim limitations. Therefore, *prima facie* obviousness has not been established for lack of evidence that the references teach all of the claim limitations. Claim 9 depends from claim 8. As such, the rejection of claims 8 and 9 should be reversed.

b. Claim 10 is fully patentable over Kablanian, Tzori, Sample and Higgins

Claim 10 depends from claim 8 and thus contains all of the limitations of claim 8. Consequently, the arguments presented above in support of the patentability of claim 8 are incorporated hereunder in support of claim 10.

Claim 10 further provides a step for listing an output of a repair program as a list of coordinates for at least one of a plurality of fuses programmed for a repair in terms of a plurality of logical addresses. The Examiner asserts that (i) a Netlist Generator block 140 and a "Part, Place, Route" block 148 in FIG. 13 of Sample and (ii) a phrase "the transistor list of layout specification is used to bu[rn] fuses" of Sample teach the claimed listing step.[43] In contrast, the blocks 140 and 148 in FIG. 13 of Sample and the above quoted phrase from Sample appear to be silent regarding a step for listing an output of a repair program as a list of coordinates for at least one of a plurality

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[42] Higging, column 1, lines 20-22.

[43] Supplemental Examiner's Answer, page 16, lines 17-21.

of fuses programmed for a repair in terms of a plurality of logical addresses as presently claimed. Furthermore, the Examiner fails to provide any evidence or convincing line of reasoning why one of ordinary skill in the art would interpret the above blocks and phrase as teaching the claim limitations. Therefore, *prima facie* obviousness has not been established for lack of evidence that the references teach all of the claim limitations. As such, the rejection of claim 10 should be reversed.

c. Claim 11 is fully patentable over Kablanian, Tzori, Sample and Higgins

Claim 11 depends from claim 10 and thus contains all of the limitations of claim 10. Consequently, the arguments presented above in support of the patentability of claim 10 are incorporated hereunder in support of claim 10.

Claim 11 further provides a step for storing coordinates in a memory. The Examiner asserts that (i) a Netlist Generator block 140 and a "Part, Place, Route" block 148 in FIG. 13 of Sample and (ii) a phrase "the transistor list of layout specification is used to bu[rn] fuses" of Sample teach the claimed step for storing.[44] In contrast, the blocks 140 and 148 in FIG. 13 of Sample and the above quoted phrase from Sample appear to be silent regarding a step for storing coordinates in a memory as presently claimed. Furthermore, the Examiner fails to provide any evidence or convincing line of reasoning why one of ordinary skill in the art would interpret the above blocks and phrase as teaching the claim limitations. Therefore, *prima facie* obviousness has not been

[44] Supplemental Examiner's Answer, page 17, lines 21-24.

established for lack of evidence that the references teach all of the claim limitations. As such, the rejection of claim 11 should be reversed.

d. Claim 17 is fully patentable over Kablanian, Tzori, Sample and Higgins

Claim 17 depends from claim 8 and thus contains all of the limitations of claim 8. Consequently, the arguments presented above in support of the patentability of claim 8 are incorporated hereunder in support of claim 17.

Claim 17 further provides a step for checking a repair file and a repair program for an error. The Examiner asserts that Tzori teaches the claimed step as follows:[45]

Various different software and hardware systems exist for simulating and/or emulating.[46]

Nowhere in the above text does Tzori appear to discuss a step for checking a repair file and a repair program for an error as presently claimed. Furthermore, the Examiner fails to provide any evidence or convincing line of reasoning why one of ordinary skill in the art would interpret the above text of Tzori as teaching the claim limitations. Therefore, *prima facie* obviousness has not been established for lack of evidence that the references teach all of the claim limitations. As such, the rejection of claim 17 should be reversed.

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[45] Supplemental Examiner's Answer, page 22, lines 9-11.

[46] Tzori, column 1, lines 17-18.

C. CONCLUSION

The Examiner has failed to establish *prima facie* obviousness for (i) lack of evidence that the references teach all of the claim limitations and (ii) lack of clear and particular motivation to combine the references. In general, the Examiner repeatedly cites the same text and the same blocks in one figure of the references regardless of the actual claim language. The Examiner also fails to show or explain why one of ordinary skill in the art would interpret the cited reference text and figures as teaching the claim limitations. Regarding the alleged motivation to combine the references, the Examiner uses a single phrase from Kablanian as motivation to combine all of the references. The single phrase from Kablanian appears to be a generic statement instead of clear and particular evidence of motivation to make the proposed combinations/modifications. As such, the new grounds of rejection should be reversed. However, should the Board find the arguments herein in support of independent claims 1, 12 and/or 13 unpersuasive, the Board is respectfully requested to carefully consider the arguments set forth above in support of each of the independently patentable groups.

Respectfully submitted,

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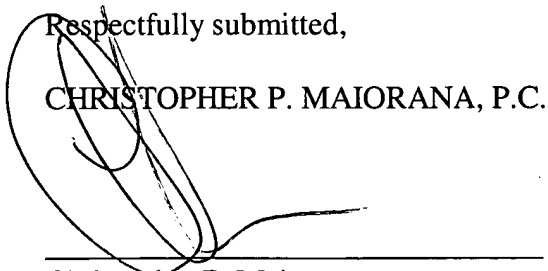

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